UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/910,088	07/20/2001	Christopher J. McCarty	00-586	2428

24319 7590 07/21/2004

LSI LOGIC CORPORATION
1621 BARBER LANE
MS: D-106 LEGAL
MILPITAS, CA 95035

EXAMINER	
PATEL, NITIN C	

ART UNIT	PAPER NUMBER
2116	2

DATE MAILED: 07/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/910,088	MCCARTY ET AL.	
	Examiner	Art Unit	
	Nitin C. Patel	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 22 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 – 2, 10 – 11, and 19 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Knight et al. [hereinafter as Knight], EP 0335812A.

4. As to claim 1, Knight discloses a system and method for booting a host adapter device [21] devoid of dedicated [without requiring] nonvolatile program memory [18, ROM], wherein said host adapter device [21] is associated with a motherboard [10, system board] having BIOS code [IPL or boot program] stored in a non-volatile memory [17, non-volatile memory], said method comprising the steps of:

a. retrieving operational programmed instructions [initialization program] for said host adapter device [21] from said non-volatile memory device [17] of said motherboard [10];

b. downloading [placing] said operational programmed instructions [initialization program] from said motherboard [10] to a volatile memory [memory space] associated with said host adapter device [10]; and

c. commencing operation [executing the initialization program] of said host adapter device executing said operational programmed instructions [initialization program] to thereby

boot said host adapter device [21] [para 57 of page 1, col. 1, lines 31 – 37, col. 2, lines 47 – 60, col. 3, lines 1 – 40], fig. 1].

5. As to claim 10, Knight discloses a system for booting a host adapter device [21] devoid of dedicated [without requiring] non-volatile program memory [ROM], wherein said host adapter device [21] is associated with a motherboard [10, system board] having BIOS code [IPL or boot program] stored in a non-volatile memory [17, non-volatile memory], said system comprising:

a. means [11, processor] for retrieving operational programmed instructions [initialization program] for said host adapter device [21] from said non-volatile memory device [17] of said motherboard [10];

b. means [11] for downloading said operational programmed instructions [initialization program] from said motherboard [10] to a volatile memory [memory space] associated with said host adapter device; and

c. means [11] for commencing operation [executing the initialization program] of said host adapter device [21] executing said operational programmed instructions [initialization program] to thereby boot said host adapter device [21] [para 57 of page 1, col. 1, lines 31 – 37, col. 2, lines 47 – 60, col. 3, lines 1 – 40], fig. 1].

6. As to claim 19, Knight discloses system [fig.1] comprising:

a. a motherboard [10, system board] including a general-purpose processor[11];

b. a nonvolatile memory [17, non-volatile storage] associated with said motherboard [10] for storing BIOS code [initialization program] to be fetched and executed by said genera-purpose processor [11];

c. a host adapter device [21] coupled to said motherboard [10] wherein said host adapter device [21] is devoid of [without requiring] nonvolatile memory [ROM] used to store operational programmed instructions [initialization program] for processing by said host adapter device [21];

d. operational programmed instructions [initialization program] stored in said nonvolatile memory [17] and used to operate said host adapter device [21]; and

e. a downloader [it is inherent to system, 10] operable on said motherboard [10] to retrieve said operational programmed instructions [initialization program] from said nonvolatile memory [17] and to download the retrieved operational programmed instructions [initialization program] to said host adapter device [21] [para 57 of page 1, col. 1, lines 31 – 37, col. 2, lines 47 – 60, col. 3, lines 1 – 40], fig. 1].

7. As to claims 2, and 11, Knight discloses the primary processor [11] for retrieving of data associated with said program instructions [the secondary processor's initialization program] from non-volatile memory device [17]; and downloading [placing] said data from motherboard [10] to volatile memory [memory space][para 57, page 1, fig.1].

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 3 – 7, 12 – 16, and 20 – 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Knight et al. [hereinafter as Knight], EP 0335812A as applied to claims 1, 10,

and 19 above, and further in view of Gillespie et al. [hereinafter as Gillespie], US Patent 5,859,987.

10. As to claims 20 – 22 Knight teaches a system and method for booting a host adapter device [20] devoid of [without requiring] nonvolatile program memory [18, ROM], wherein said host adapter device [21] is associated with a motherboard [10, system board] having BIOS code [IPL or boot program] stored in a non-volatile memory [17, non-volatile memory] by retrieving operational programmed instructions [initialization program] for said host adapter device [21] from said non-volatile memory device [17] of said motherboard [10]; downloading [placing] said operational programmed instructions [initialization program] from said motherboard [10] to a volatile memory [memory space] associated with said host adapter device [10]; and commencing operation [executing the initialization program] of said host adapter device executing said operational programmed instructions [initialization program] to thereby boot said host adapter device [21] [para 57 of page 1, col. 1, lines 31 – 37, col. 2, lines 47 – 60, col. 3, lines 1 – 40], fig. 1].

However, Knight does not explicitly teach that a system bus [19] for coupling the motherboard [10] to the host adapter [20] to makes an integral with motherboard [10] is a PCI bus.

Gillespie discloses a computer system with a host adapter [PCI compliant Intelligent Computer Add-in card, 41] coupled to a PCI bus slot [5] disposed on a motherboard [fig. 2, 3] which devoid [obviates the need] for non-volatile memory [Read Only Memory [ROM]] by allowing host processor to initialize the embedded system and also download code from a host memory to the embedded RAM in subsystem [col. 3, lines 17 – 23].

It would have been obvious to one of ordinary skill in art, having teachings of Knight and Gillespie before him at the time of invention was made, to modify the system bus coupling of host adapter [20] to the motherboard [10] disclosed by Knight to include a PCI bus for coupling of host adapter to motherboard as taught by Gillespie, in order to obtain a host adapter to make an integral with motherboard that controls the reset sequence of the intelligent I/O subsystem on the intelligent bridge and guarantees the synchronization of the initialization sequence between the integrated processor in the intelligent bridge and the host processor [col. 3, lines 24 – 28].

11. As to claims 3 – 7, and 12 – 16, Gillespie teaches computer system motherboard and coupling of host adapter on PCI bus slot with PCI bus operations including initialization and reset, therefore, he teaches procedural steps involved in operations according to PCI bus standard and specifications.

12. Claims 8 – 9, and 17 – 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Knight et al. [hereinafter as Knight], EP 0335812A, and further in view of Gillespie et al. [hereinafter as Gillespie], US Patent 5,859,987, over Knight et al. [hereinafter as Knight], EP 0335812A as applied to claims 1 - 7, and 10 - 16, above, and further in view of Leung et al. [hereinafter as Leung], US Patent 6,446,139.

13. As to claims 8 – 9, and 17 – 18 Knight teaches a system and method for booting a host adapter device [20] devoid of [without requiring] nonvolatile program memory [18, ROM], wherein said host adapter device [21] is associated with a motherboard [10, system board] having BIOS code [IPL or boot program] stored in a non-volatile memory [17, non-volatile memory] by retrieving operational programmed instructions [initialization program] for said host adapter device [21] from said non-volatile memory device [17] of said motherboard [10];

downloading [placing] said operational programmed instructions [initialization program] from said motherboard [10] to a volatile memory [memory space] associated with said host adapter device [10]; and commencing operation [executing the initialization program] of said host adapter device executing said operational programmed instructions [initialization program] to thereby boot said host adapter device [21] [para 57 of page 1, col. 1, lines 31 – 37, col. 2, lines 47 – 60, col. 3, lines 1 – 40], fig. 1].

However, Knight does not explicitly teach that a system bus [19] for coupling the motherboard [10] to the host adapter [20] to makes an integral with motherboard [10] is a PCI bus and uploading operational program instructions from volatile memory in host adapter device to a memory in motherboard [generated option ROM code flashed to the system ROM] and different steps involved in it.

Gillespie discloses a computer system with a host adapter [PCI compliant Intelligent Computer Add-in card, 41] coupled to a PCI bus slot [5] disposed on a motherboard [fig. 2, 3] which devoid [obviates the need] for non-volatile memory [Read Only Memory [ROM]] by allowing host processor to initialize the embedded system and also download code from a host memory to the embedded RAM in subsystem [col. 3, lines 17 – 23].

Leung teaches a computer system with motherboard [200] having a system BIOS in system ROM [204] and plurality of host adapters [HA] coupled to different PCI slots on motherboard [200] with a PCI bus [fig. 1A] also teaches to upload [to flash] generated modified option ROM code to the system ROM [204][col. 5, lines 10 – 18].

It would have been obvious to one of ordinary skill in art, having teachings of Knight and Gillespie before him at the time of invention was made, to modify the system bus coupling of

host adapter [20] to the motherboard [10] disclosed by Knight to include a PCI bus for coupling of host adapter to motherboard as taught by Gillespie, and Leung 's method for uploading operational instructions from volatile memory in host device to a memory in motherboard [system ROM] in order to obtain a host adapter to make an integral with motherboard that controls the reset sequence of the intelligent I/O subsystem on the intelligent bridge and guarantees the synchronization of the initialization sequence between the integrated processor in the intelligent bridge and the host processor [col. 3, lines 24 – 28] and one BIOS image can control a set of controller chips that may be integrated as apart of a computer system's motherboard [col. 3, lines38 – 41].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin C. Patel whose telephone number is 703-305-3994. The examiner can normally be reached on 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Brown can be reached on 703-308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nitin C. Patel
July 13, 2004

LYNNE H. BROWNE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER ~~3600~~ 2100